LAN9221/LAN9221i

High-Performance 16-bit Non-PCI 10/100 Ethernet Controller with Variable Voltage I/O

PRODUCT FEATURES

Data Brief

Highlights

- Optimized for high performance applications
- Efficient architecture with low CPU overhead
- Easily interfaces to most 16-bit embedded CPU's
- 1.8V to 3.3V variable voltage I/O accommodates wide range of I/O signalling without voltage level shifters
- Integrated PHY with HP Auto-MDIX support
- Integrated checksum offload engine helps reduce CPU load
- Low pin count and small body size package for small form factor system designs

Target Applications

- Cable, satellite, and IP set-top boxes
- Digital video recorders and DVD recorder/players
- Digital TV
- Digital media clients/servers and home gateways
- Video-over IP solutions, IP PBX & video phones
- Wireless routers & access points
- High-end audio distribution systems

Key Benefits

- Non-PCI Ethernet controller for high performance applications
  - 16-bit interface with fast bus cycle times
  - Burst-mode read support
- Minimizes dropped packets
  - Internal buffer memory can store over 200 packets
  - Automatic PAUSE and back-pressure flow control
- Minimizes CPU overhead
  - Supports Slave-DMA
  - Interrupt Pin with Programmable Hold-off timer
- Reduces system cost and increases design flexibility
- SRAM-like interface easily interfaces to most embedded CPU's or SoC'sReduced Power Modes
  - Numerous power management modes
  - Wake on LAN
  - Magic packet wakeup
  - Wakeup indicator event signal
  - Link Status Change
- Single chip Ethernet controller
  - Fully compliant with IEEE 802.3/802.3u standards
  - Integrated Ethernet MAC and PHY
  - 10BASE-T and 100BASE-TX support
  - Full- and Half-duplex support
  - Full-duplex flow control
  - Backpressure for half-duplex flow control
  - Preamble generation and removal
  - Automatic 32-bit CRC generation and checking
  - Automatic payload padding and pad removal
  - Loop-back modes
- Flexible address filtering modes
  - One 48-bit perfect address
  - 64 hash-filtered multicast addresses
  - Pass all multicast
  - Promiscuous mode
  - Inverse filtering
  - Pass all incoming with status report
  - Disable reception of broadcast packets
- Integrated 10/100 Ethernet PHY
  - Supports HP Auto-MDIX
  - Auto-negotiation
  - Supports energy-detect power down
- Host bus interface
  - Simple, SRAM-like interface
  - 16-bit data bus
  - 16Kbyte FIFO with flexible TX/RX allocation
  - One configurable host interrupt
- Miscellaneous features
  - Small form factor, 56-pin QFN lead-free RoHS Compliant package
  - Integrated 1.8V regulator
  - Integrated checksum offload engine
  - Mixed endian support
  - General Purpose Timer
  - Optional EEPROM interface
  - Support for 3 status LEDs multiplexed with Programmable GPIO signals
- Single 3.3V Power Supply with Variable Voltage I/O
- Commercial and Industrial Temperature Support

ORDER NUMBER(S):

LAN9221-ABZJ FOR 56-PIN, QFN LEAD-FREE ROHS COMPLIANT PACKAGE (0 TO +70°C TEMP RANGE)

LAN9221i-ABZJ FOR 56-PIN, QFN LEAD-FREE ROHS COMPLIANT PACKAGE (-40 TO +85°C TEMP RANGE)

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000, FAX (631) 273-3123

General Description

The LAN9221/LAN9221i is a full-featured, single-chip 10/100 Ethernet controller designed for embedded applications where performance, flexibility, ease of integration and system cost control are required. The LAN9221/LAN9221i has been specifically designed to provide high performance and throughput for 16-bit applications. The LAN9221/LAN9221i is fully IEEE 802.3 10BASE-T and 802.3u 100BASE-TX compliant, and supports HP Auto-MDIX. The variable voltage I/O signals of the LAN9221/LAN9221i accommodate lower voltage I/O signalling without the need for voltage level shifters.

The LAN9221/LAN9221i includes an integrated Ethernet MAC and PHY with a high-performance SRAM-like slave interface. The simple, yet highly functional host bus interface provides a glue-less connection to most common 16-bit microprocessors and microcontrollers as well as 32-bit microprocessors with a 16-bit external bus. The integrated checksum offload engines enable the automatic generation of the 16-bit checksum for received and transmitted Ethernet frames, offloading the task from the CPU. The LAN9221/LAN9221i also includes large transmit and receive data FIFOs to accommodate high latency applications. In addition, the LAN9221/LAN9221i memory buffer architecture allows highly efficient use of memory resources by optimizing packet granularity.

Applications

The LAN9221/LAN9221i is well suited for many high-performance embedded applications, including:

- Cable, satellite and IP set-top boxes
- High-end audio distribution systems
- Digital video recorders
- DVD Recorders/Players
- Digital TV
- Digital media clients/servers
- Home gateways
- Industrial and embedded systems with extended temperature support

The LAN9221/LAN9221i also supports features which reduce or eliminate packet loss. Its internal 16-KByte SRAM can hold over 200 received packets. If the receive FIFO gets too full, the LAN9221/LAN9221i can automatically generate flow control packets to the remote node, or assert back-pressure on the remote node by generating network collisions.

The LAN9221/LAN9221i supports numerous power management and wakeup features. The LAN9221/LAN9221i can be placed in a reduced power mode and can be programmed to issue an external wake signal via several methods, including “Magic Packet”, “Wake on LAN” and “Link Status Change”. This signal is ideal for triggering system power-up using remote Ethernet wakeup events. The device can be removed from the low power state via a host processor command.

Block Diagram

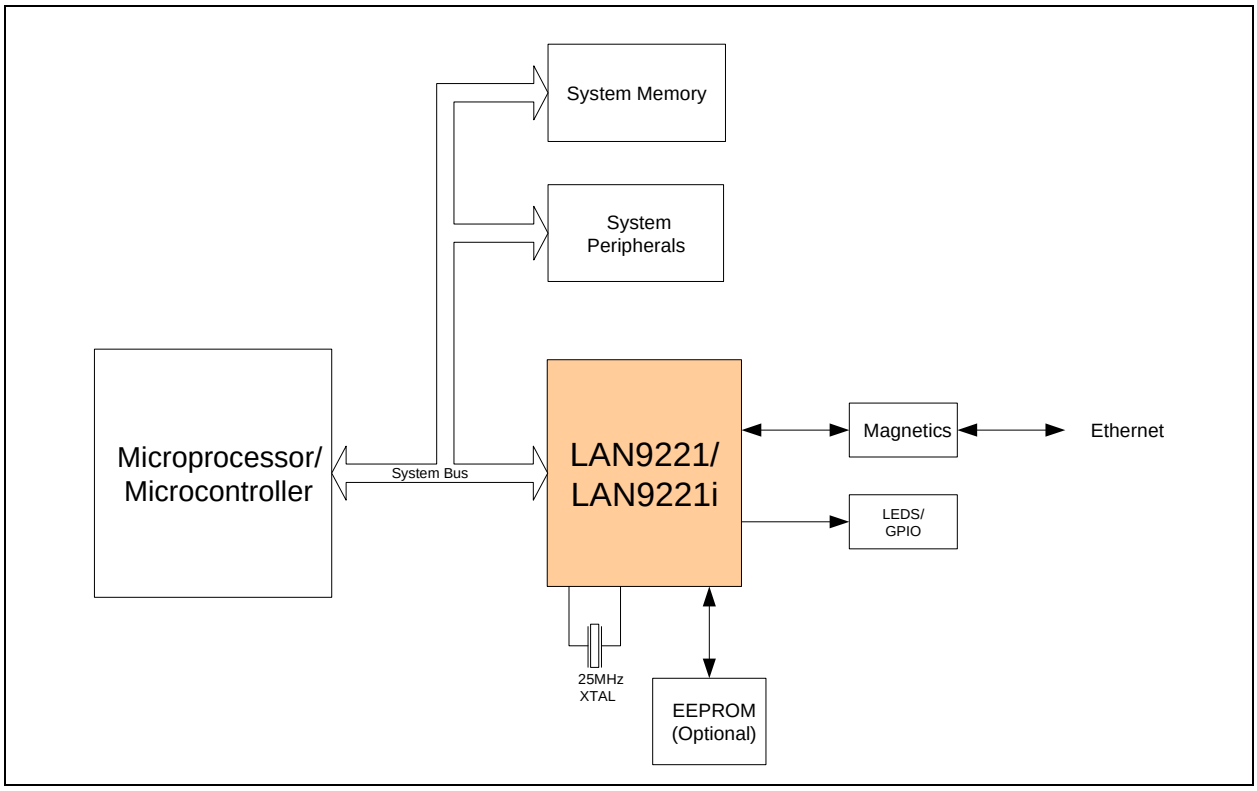


Figure 1 System Block Diagram

Package Outline

56-QFN Package

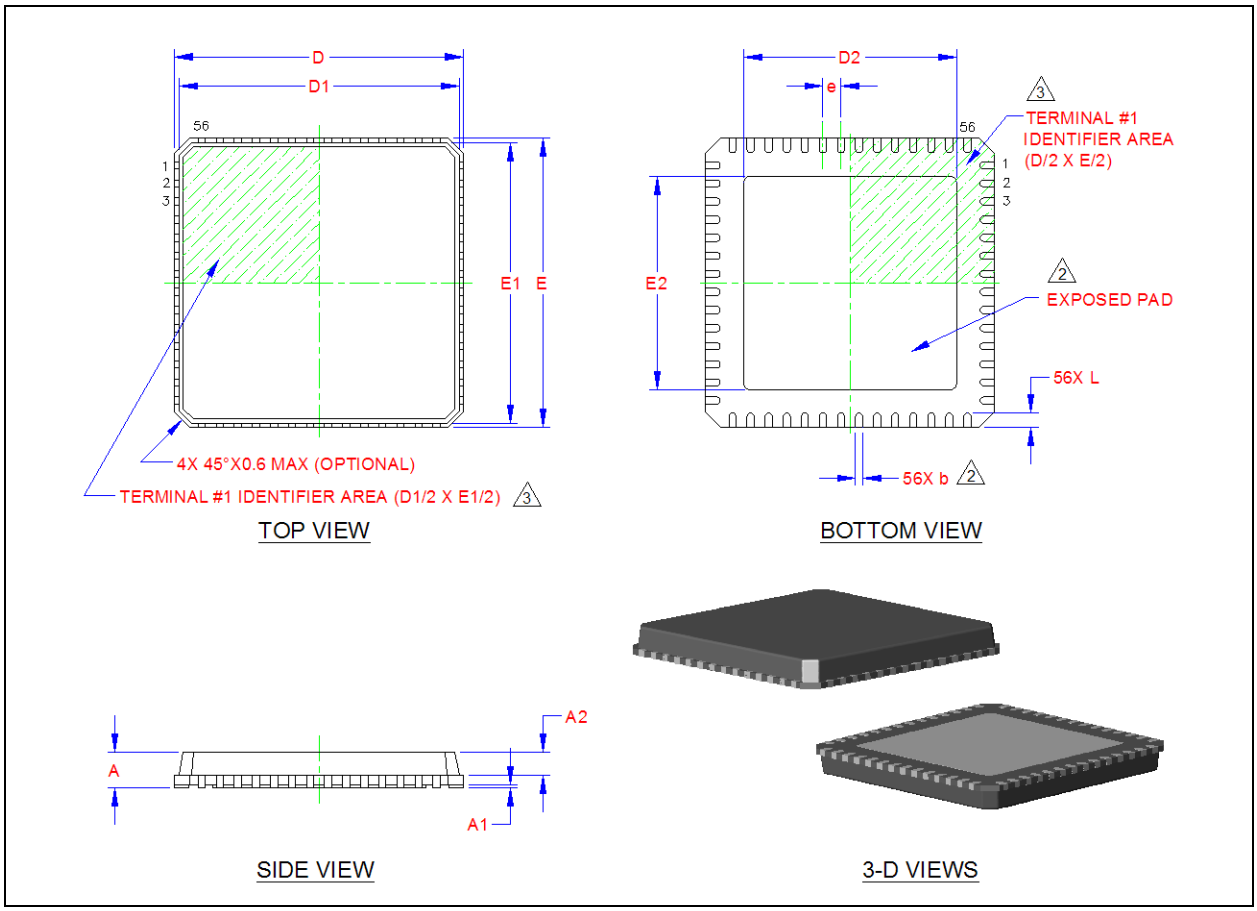


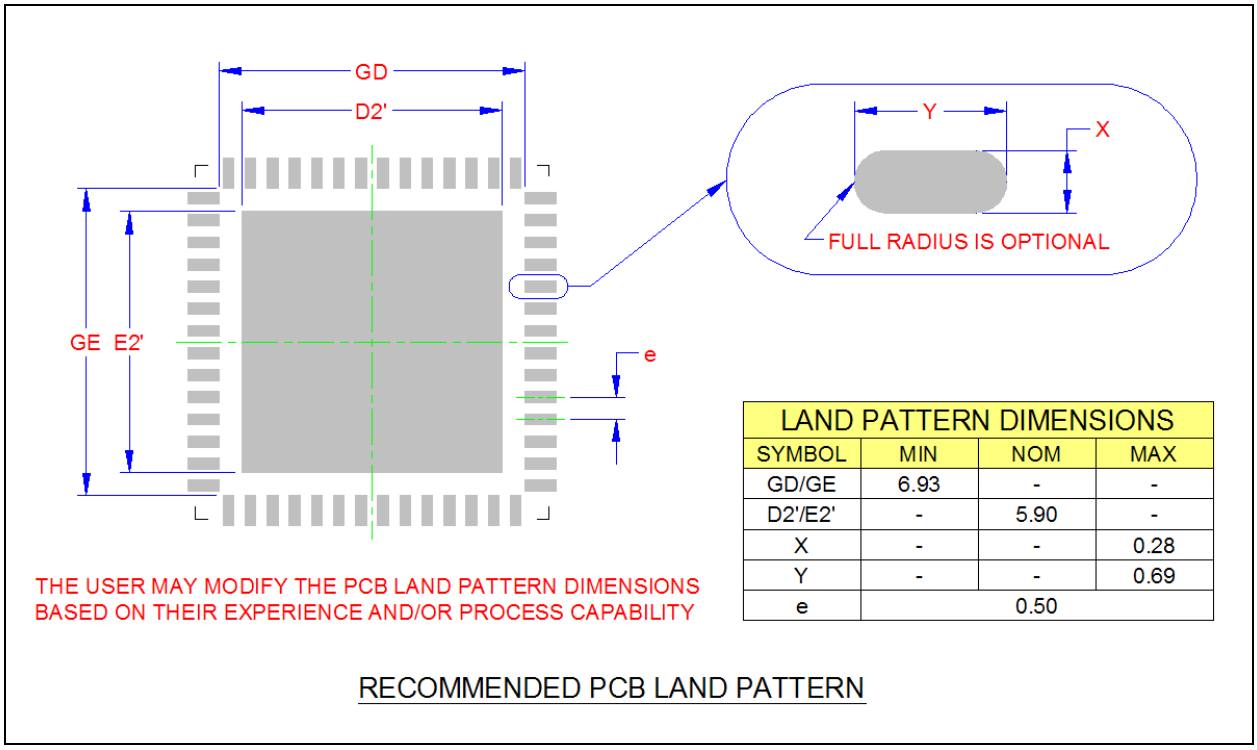
Figure 2 56-Pin QFN Package Definition

Table 1 56-Pin QFN Package Parameters

	MIN	NOMINAL	MAX	REMARKS
A	0.70	~	1.00	Overall Package Height
A1	0.00	0.02	0.05	Standoff
A2	~	~	0.90	Mold Cap Thickness
D/E	7.85	8.00	8.15	X/Y Body Size
D1/E1	7.55	~	7.95	X/Y Mold Cap Size
D2/E2	5.75	5.90	6.05	X/Y Exposed Pad Size
L	0.30	~	0.50	Terminal Length
b	0.18	0.25	0.30	Terminal Width
e	0.50 Basic			Terminal Pitch

Notes:

1. All dimensions are in millimeters.
2. Position tolerance of each terminal and exposed pad is ± 0.05 mm at maximum material condition. Dimension “b” applies to plated terminals and is measured between 0.15 and 0.30 mm from the terminal tip.
3. The pin 1 identifier may vary, but is always located within the zone indicated.



LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
GD/GE	6.93	-	-
D2'/E2'	-	5.90	-
X	-	-	0.28
Y	-	-	0.69
e		0.50	

Figure 3 56-Pin QFN Recommended PCB Land Pattern