ISEE IGEPv2 BOARD

IGEPv2 BOARD
Hardware Reference Manual
(Revision 1.13)

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VERSION CONTROL

REVISIÓN	DATE	ORIGIN	DESCRIPTION
1.00	19/03/09	R&D	Initial version
1.02	20/05/09	R&D	Board Configuration update.
1.10	24/07/09	R&D	Update Hw Revision RB1
1.11	21/09/09	R&D	Document Update
1.12	24/09/09	R&D	Document Update
1.13	23/10/09	R&D	Document Update

1 COPYRIGHT NOTICE

2 WARRANTY

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund.

THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies ISEE 2007 SL from all claims arising from the handling or use of the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

ISEE 2007 SL currently deals with a variety of customers for products, and therefore our arrangement with the user is not exclusive. ISEE assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein.

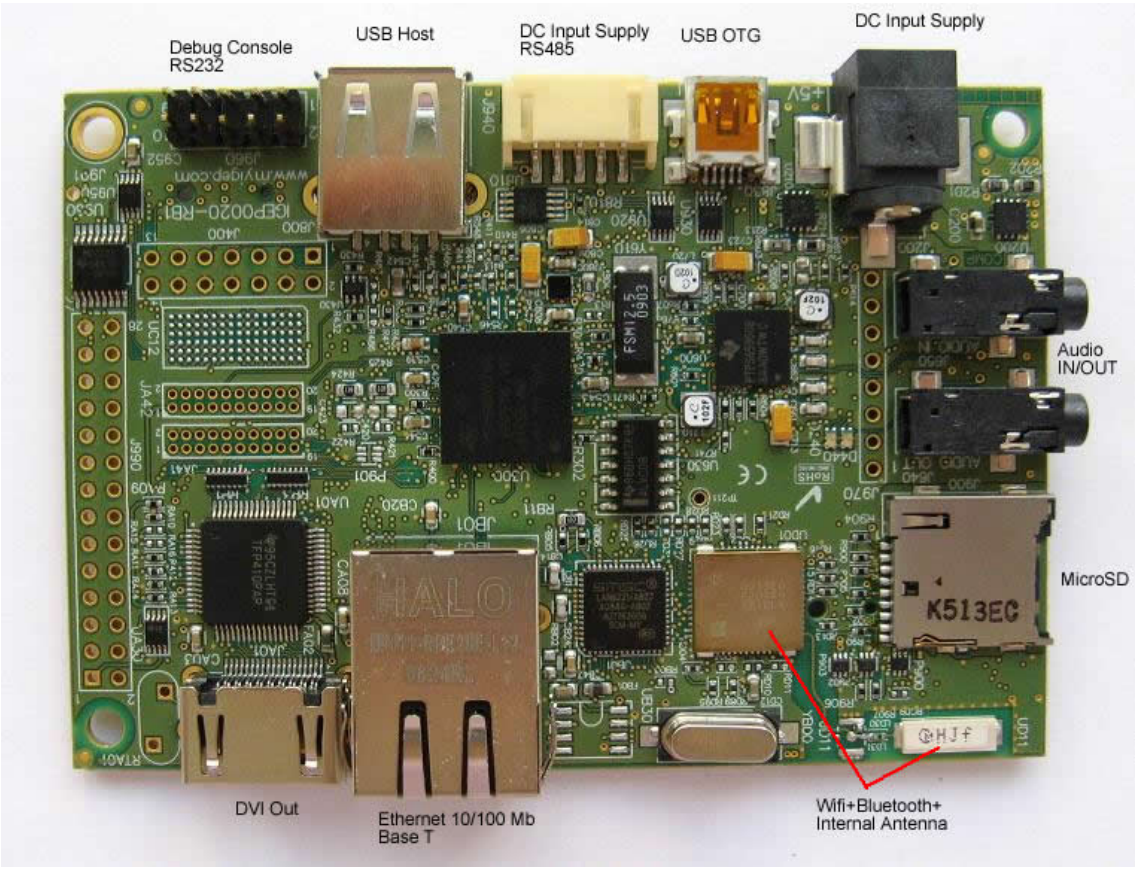
Please read specifically, the Warnings and Restrictions notice in this manual prior to handling the product. This notice contains important safety information about

temperatures and voltages. For additional information on IGEPV2 environmental and/or safety programs, please contact with ISEE (support@iseebcn.com).

No license is granted under any patent right or other intellectual property right of ISEE covering or relating to any machine, process, or combination in which such ISEE products or services might be or are used.

WARRANTY: IGEPV2 is warranted against defects in materials and workmanship for a period of 1 year from purchase. This warranty does not cover any problems occurring as a result of improper use, modifications, exposure to water, excessive voltages, abuse, or accidents. All boards will be returned via standard mail if an issue is found. If no issue is found or express return is needed, the customer will pay all shipping costs.

3 ISEE IGEPV2 BOARD FEATURES



Description	Characteristics
Processor	OMAP3530 (ARM Cortex-A8)
Processor Speed	600 Mhz
Memory SDRAM	512 MBytes LPDDR SDRAM – 200 Mhz
Nand Flash	512 Mbytes
DSP	TMS320DM64+
DSP Speed	430 Mhz
Video 3D Accelerator	PowerVR SGX 530
Power Management	TPS65950
Debug	Console RS232 + JTAG Interface

PCB size	93 x 65 x 1.6 mm
Indicators	2 Bicolor USER LEDS
USB 2.0 LS/FS/HS OTG	1 Mini AB USB socket connector (dual slave and host role)
USB 2.0 HS HOST	1 Type A USB socket connector (standard USB host)
Audio stereo in/out	3.5mm standard stereo audio jack
microSD	microSD connector (SD and SDHC cards supported)
DVI video output	DVI-D using HDMI connector. (video and TS lines are available in expansion connector also).
Power	5Vcc / 1A 3.5mm socket connector for wall plug or JST Connector
Expansion connector	Power 5V and 1.8V, UART, McBSP, McSPI, I2C, GPIO, RS485 with transceiver, Keyboard.
Wifi	IEEE 802.11b/g 2,4GHz
Bluetooth	2.0
Antenna WiFi/Bluetooth	1 shared internal antenna (integrated on PCB)
Ethernet	10/100 MB BaseT (RJ45 connector with led link/activity)
Temperature Range	Industrial range (-40 to +80 Cº Degrees)

WARNING: IGEPv2 BOARD CAN ONLY BE POWERED WITH 5V DC POWER SUPPLY OR THE BOARD WILL BE DAMAGED!

The following sections provide more detail on each feature and components on the IGEPv2 BOARD.

3.1 ISEE IGEPV2 BOARD GENERAL SPECIFICATIONS

OMAP Processor

The IGEPv2 BOARD uses the OMAP3530 version ES3.1 and comes in a .4mm pitch memory POP package on it.

POP (Package on Package) is a technique where the memory, NAND and SDRAM, are mounted on top of the OMAP3530. For this reason, when looking at the IGEPv2 BOARD, you will not find an actual part labeled OMAP3530.

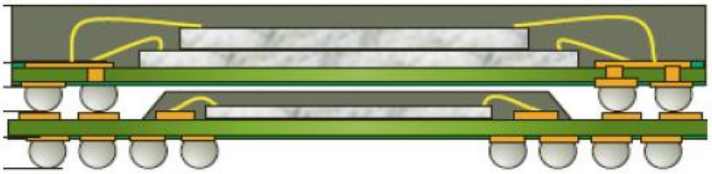


Figure 1 POP Package

Memory

The memory is mounted on top of the processor as mentioned. The key function of the POP memory is to provide:

- 4Gb NAND x 16 (512MB)
- 4Gb LP-DDR SDRAM x32 (512MB @ 200MHz)

Power Management

The TPS65950 is used on the board to provide power to the IGEPv2 Board with the exception of the 3.3V regulator which is used to provide power to the DVI-D encoder and RS232 driver. In addition to the power it also provides:

- Stereo Audio Out
- Stereo Audio in
- Power on reset
- USB OTG PHY
- Status LED

USB 2.0 LS/FS/HS OTG

On the board a single USB 2.0 OTG Port is provided.

Figure 2 USB OTG connector

It is not possible to power the board with the OTG connector.

USB 2.0 HS HOST

On the board a single USB 2.0 HS HOST only one port is provided via a USB Type A socket connector. Hardware provides power on/off switch control and up to 500mA of current limit at 5V.

Figure 3 USB HOST connector

USB HOST Port supports only high speed devices (USB 2.0 HS devices). In order to support low speed devices (USB 1.0 LS devices) or full speed devices (USB 1.1 FS devices), external USB 2.0 HUB must be used.

WIFI

IEEE802.11b/g compliant.

Chipset based on Marvell 88W8686. The 88W8686 integrates a dual-band RF transceiver operating at 2.4 and 5 GHz, a physical layer, a media access controller, and an ARM processor into a single die.

BLUETOOTH

Bluetooth 2.0 compliant.

Class 2, 2.5 mW (4 dBm) ~10 meters

Version 2.0 + EDR 3 Mbit/s

ETHERNET

On board a RJ45 connector is provided for the Ethernet 10/100 Base T interface.

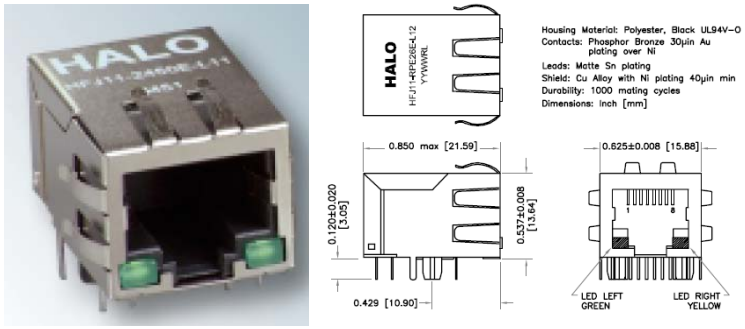


Figure 4 ETHERNET connector

This connectors comes with link and activity status led.

Stereo Audio Output Connector

A 3.5mm standard stereo output audio jack is provided to access the stereo output of the onboard audio CODEC. The Audio CODEC is provided by the TPS65950.

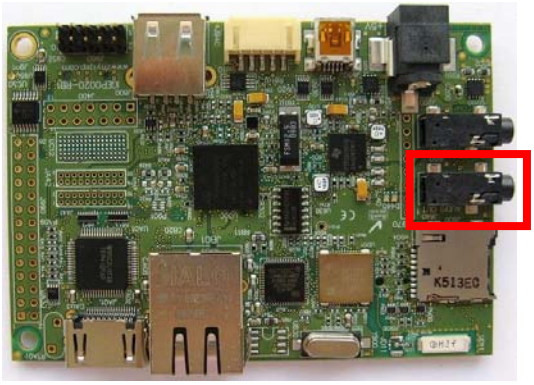


Figure 5 Stereo Output connector location

Stereo Audio In connector

A 3.5mm standard stereo audio input jack is provided to access the stereo input of the onboard audio CODEC.

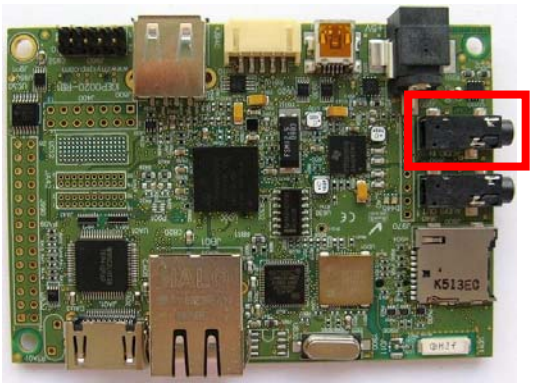


Figure 6 Stereo Input connector location

DVI-D Connector

The IGEPv2 BOARD can drive a LCD panel equipped with a DVI-D digital input. This is the standard LCD panel interface of the OMAP3530.

Figure 7 HDMI connector

DDC2B (Display Data Channel) or EDID (Enhanced Display ID) support over I2C is provided in order to allow for the identification of the LCD monitor type and settings.

The IGEPv2 BOARD does not support the full HDMI interface and is used to provide the DVI-D interface portion only. The user must use a HDMI to DVI-D cable or adapter to connect to a LCD monitor. A standard HDMI cable can be used when connecting to a monitor with and HDMI connector.

LCD and touchscreen header

A pair of 1.27mm pitch 2x10 headers are provided to gain access to the LCD signals and touchscreen control.

This allows for the creation of LCD boards that will allow adapters to be made to provide the level translation to support different LCD panels.

microSD Connector

A microSD connector is provided for microSD cards form factor.

The microSD memory card is the smallest memory card available commercially, with the lowest price per capacity and the highest capacity. At 15 mm × 11 mm × 1 mm (about the size of a fingernail), it is about a quarter the size of an SD card.

The microSD connector supports SD and SDHC cards. SDHC (Secure Digital High Capacity, SD 2.0) is an extension of the SD standard which increases card's storage capacity up to 32GB. SDHC cards shares the same physical and electrical form factor as older (SD 1.x) cards, allowing SDHC-devices to support both newer SDHC cards and older SD-cards.

Indicators

There are two bicolor LEDs on the Board that can be controlled by the user.

- First one is programmed via the I2C interface on the TPS65950
- Second one is controlled via GPIO pins on the OMAP3530 Processor

Power Connector

Power will be supplied via the DC power jack (or via JST connector).

JTAG Connector

A 14 pin JTAG header is provided on the board to facilitate the SW development and debugging of the board by using various JTAG emulators. The interface is at 1.8V on all signals. Only 1.8V CMOS levels are supported. **DO NOT expose the JTAG header to 3.3V.**

Expansion Header

An option for a single 28 pin header is provided on the board to allow for the connection of various expansion cards that could be developed by the users or other sources. Due to multiplexing, different signals can be provided on each pin providing more that 24 actual signal accesses.

3.2 SYSTEM BLOCK DIAGRAM

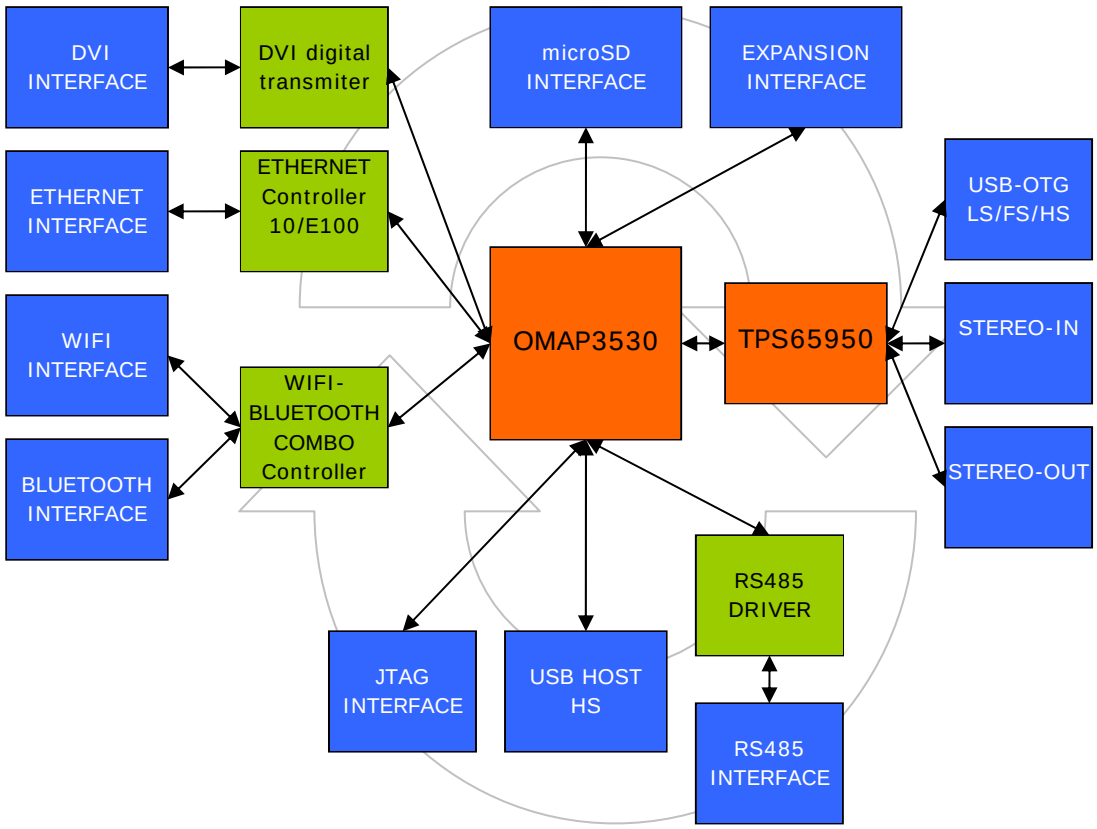


Figure 8 IGEPv2 BOARD high level block diagram

3.3 GENERAL VIEW

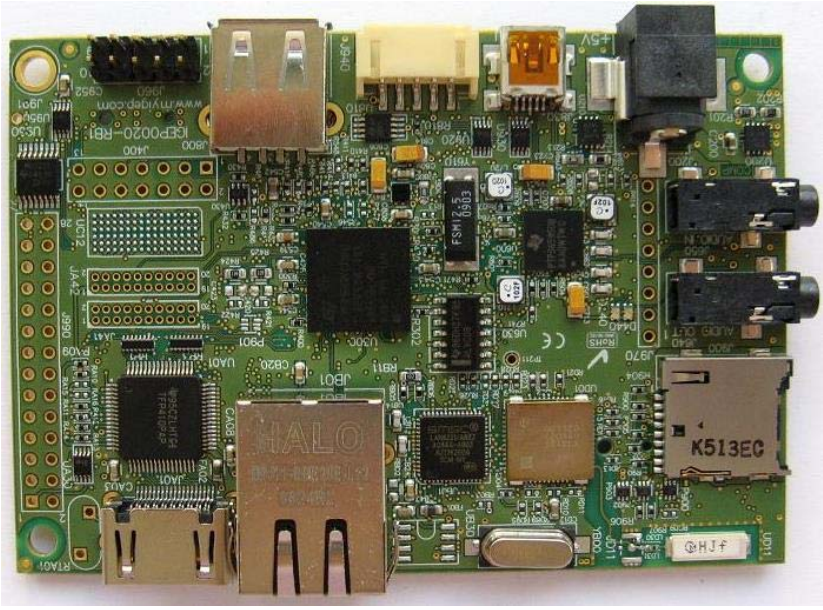


Figure 9 IGEPv2 BOARD top side components

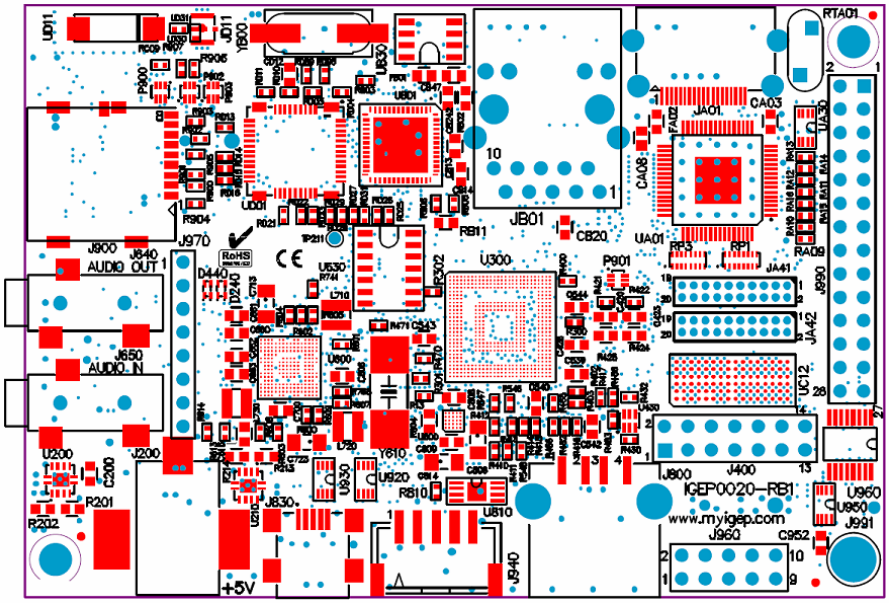


Figure 10 IGEPv2 BOARD top side components

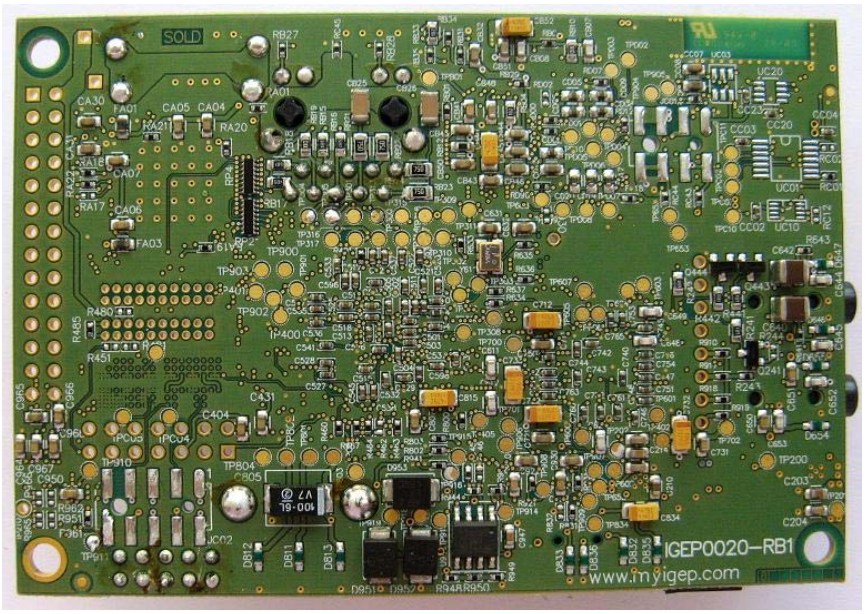


Figure 11 IGEPv2 BOARD bottom side components

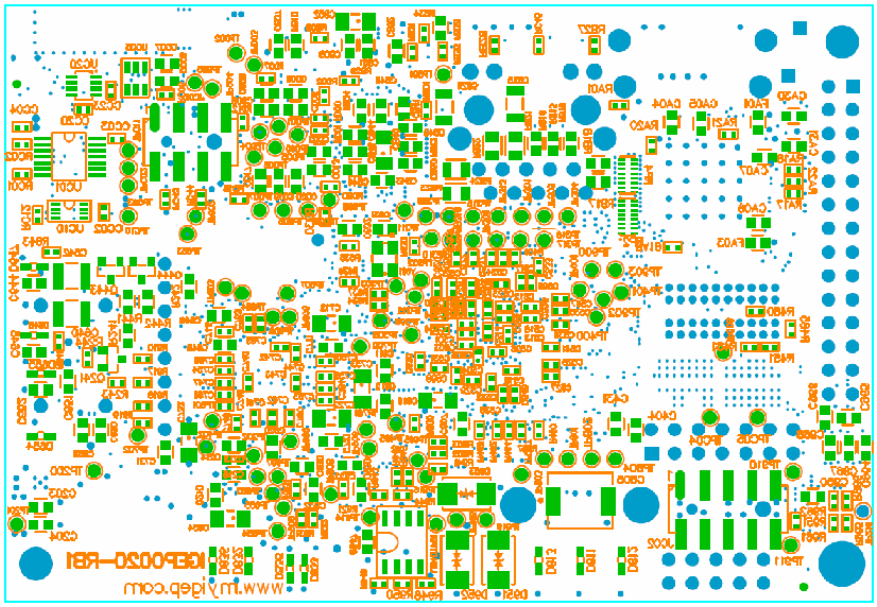


Figure 12 IGEPv2 BOARD bottom side components

3.4 MECHANICAL SPECIFICATION

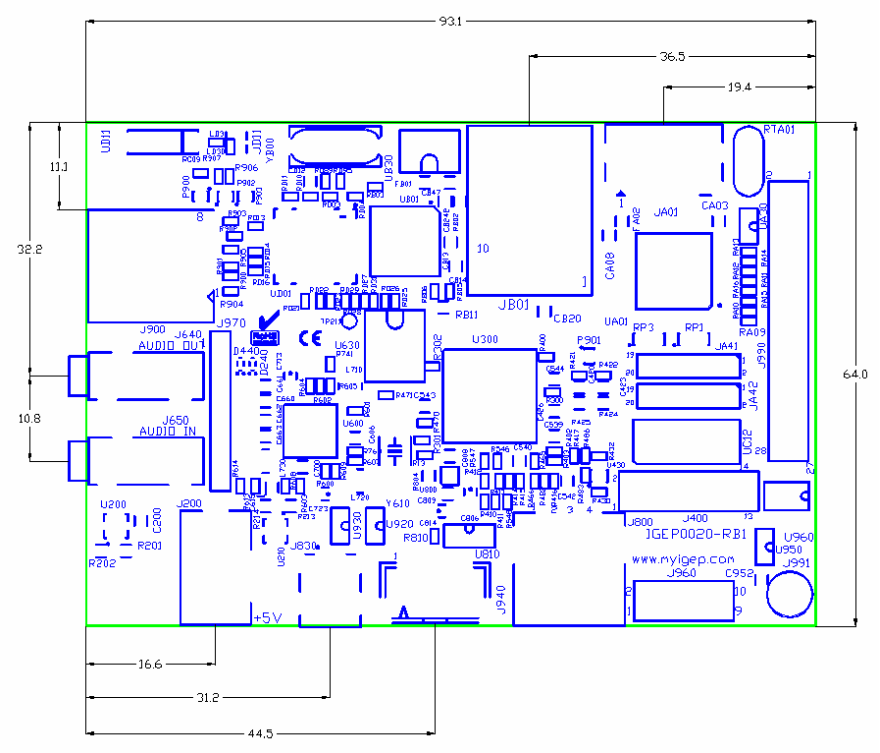


Figure 13 Top view mechanical specification

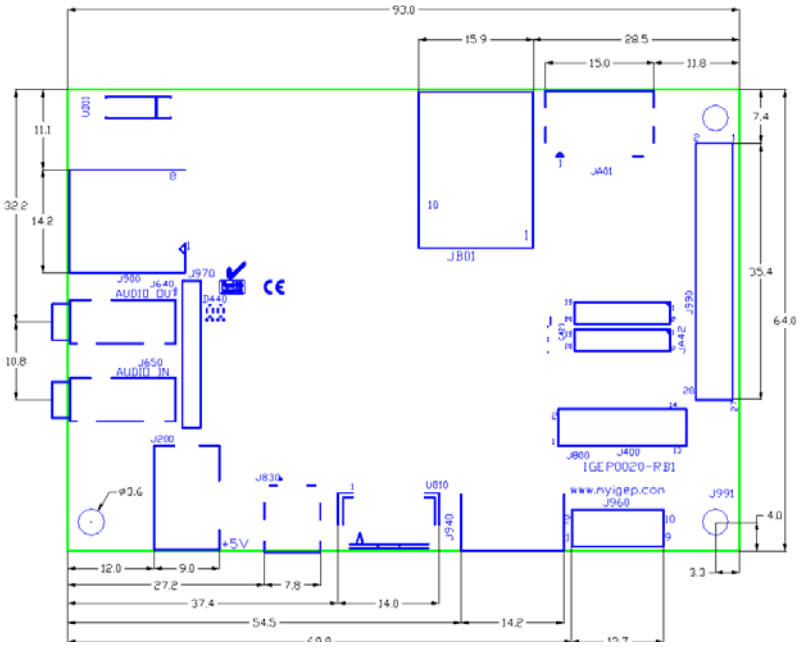


Figure 14 Top view mechanical specification

3.5 ELECTRICAL SPECIFICATIONS

Specification	Min	Typ	Max	Unit
Power				
Input Voltage DC	4.8	5	5.2	V
Current DC		1000		mA
USB 2.0 OTG				
High Speed Mode (HS)			480	Mb/s
Full Speed Mode (FS)			12.5	Mb/s
Low Speed Mode (LS)			1.5	Mb/s
USB 2.0 Host				
High Speed Mode (HS)			480	Mb/s
RS485				
Driver				
Input High Voltage	2			V
Input Low Voltage			0.8	V
Maximum Data Rate	250			Kbps
Receiver				
Output Voltage High	2.8			V
Output Voltage Low			0.4	V
Input Resistance	12	15		KOhms
JTAG				
Realview ICE Tool			30	MHz
XDS560			30	MHz
XDS510			30	MHz
Lauterbach(tm)			30	MHz
microSD				
Voltage Mode 1.8V	1.71	1.8	1.89	
Voltage Mode 3.3V	3.2	3.3		
Current			220	mA
Clock			48	MHz
DVI-D				
Pixel Clock Frequency	25		65	MHZ
High level output voltage		3.3		V
Swing output voltage	400		600	mVp-p
Maximum resolution	67.5	75	82.5	Ohms
Audio-In				
Peak-to-peak single-ended input voltage (0 dBFs)			1.5	Vpp
Total harmonic distortion (sine wave @ 1.02 kHz @ -1 dBFs)		-80	-75	dB
Total harmonic distortion (sine wave @ 1.02 kHz) 20 Hz to 20 kHz, A-weighted audio, Gain = 0 dB		-85	-78	dB
Audio-Out				
Load Impedance @100 pF	14	16		Ohms
Maximum Output Power (At 0.53 Vrms differential output voltage and load impedance = 16 Ohms)		17.56		mW
Peak-to-Peak output voltage			1.5	Vpp

Total Harmonic Distortion @ 0 dBFs		-80	-75	dB
Idle channel noise (20Hz to 20KHz)		-90	-85	dB
Ethernet				
Fully compliant with IEEE 802.3/802.3u				
10BASE-T and 100BASE-TX support				
Power supply		3.3		V
Wifi IEEE802.11b				
Specification		IEEE802.11b		
Frequency 2400 - 2500MHz	2400		2500	MHz
Data rate		1, 2, 5.5, 11		Mbps
Power Levels	15.5	17.5	19.5	dBm
Minimum Input Level Sensitivity 11Mbps (FER < 8%)	-	-87	-81	dBm
Maximum Input Level	-10	-5	-	dBm
Wifi IEEE802.11g				
Specification		IEEE802.11g		
Frequency 2400 - 2500MHz	2400		2483.5	MHz
Data rate		6, 9, 12, 18, 24, 36, 48, 54		Mbps
Power Levels	13	14.8	17.0	dBm
Minimum Input Level Sensitivity 11Mbps (FER < 8%)	-	-71	-65	dBm
Maximum Input Level	-20	-15	-	dBm
Bluetooth 2.0				
Bluetooth specification		2.0		
Channel spacing		1		MHz
Output Power	-4	0	+4	dBm
Frequency range (Rx/Tx)	2400		2483.5	MHz
Sensitivity (BER 0.1%)				
1) 2402MHz - -81 -73 dBm	-	-81	-73	dBm
2) 2441MHz	-	-81	-73	dBm
3) 2480MHz	-	-79.5	-73	dBm
C/I Performance (BER 0.1%)				
1) co-channel ratio (-60dBm input)	-	7.6	11	dBm
2) 1MHz ratio (-60dBm input)	-	-2.5	0	dBm
3) 2MHz ratio (-60dBm input)	-	-42.6	-30	dBm

4 CONNECTORS DESCRIPTION

This section will guide you through the ISEE IGEPv2 BOARD expansion connectors:

- Connector J200: main Power
- Connector J400: JTAG DEBUG
- Connector J940: Power + RS485
- Connector J960: Serial Debug
- Connector J940: Keyboard Matrix 4x4
- Connector JA41-JA42: External TFT interface
- Connector J990: GPIO
- Connector JC01: AD
- Connector JD11: External Wifi Antenna

4.1 CONNECTOR J200: MAIN 5.0VCC POWER

The J200 connector is a power jack for main 5 VDC power.

It is a RASM722 switchcraft connector, Plug/Mating Plug Diameter 2.1mm ID, 5.5mm OD.

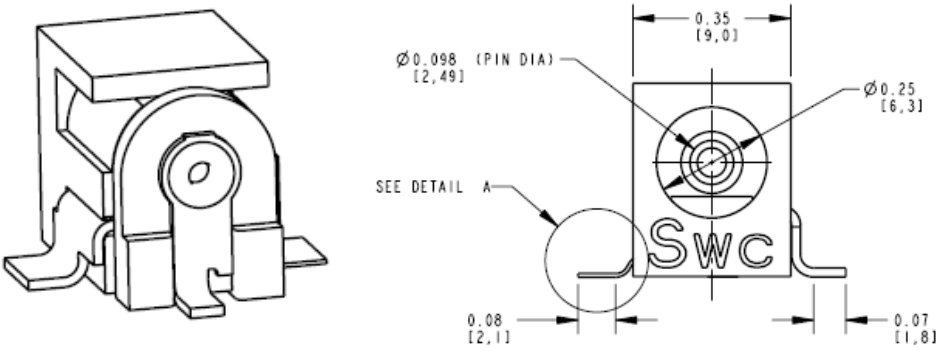


Figure 15 J200 detail

WARNING: IGEPv2 BOARD CAN ONLY BE POWERED WITH 5V DC POWER SUPPLY OR THE BOARD WILL BE DAMAGED!

4.2 CONNECTOR J400: JTAG DEBUG

The J400 connector is a 14 pins 2x7 dual row 2.54mm.

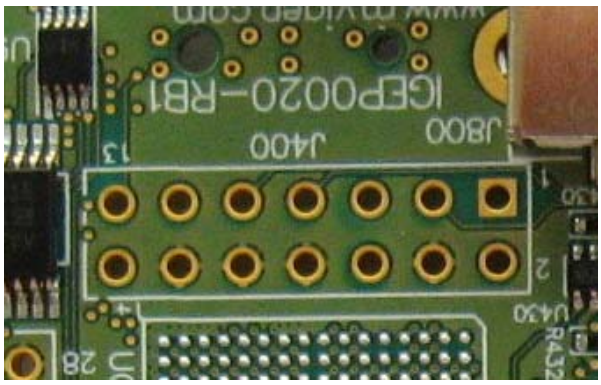


Figure 16 J400 detail

Pins 1, 2, 13 and 14 are labeled on the PCB. The connector is located as shows the figure below.

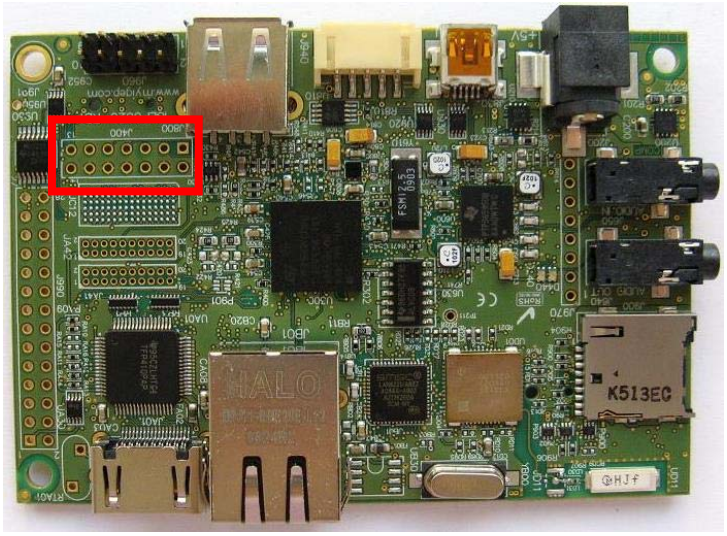


Figure 17 J400 location

The schematic below illustrate the pinout of the connector.

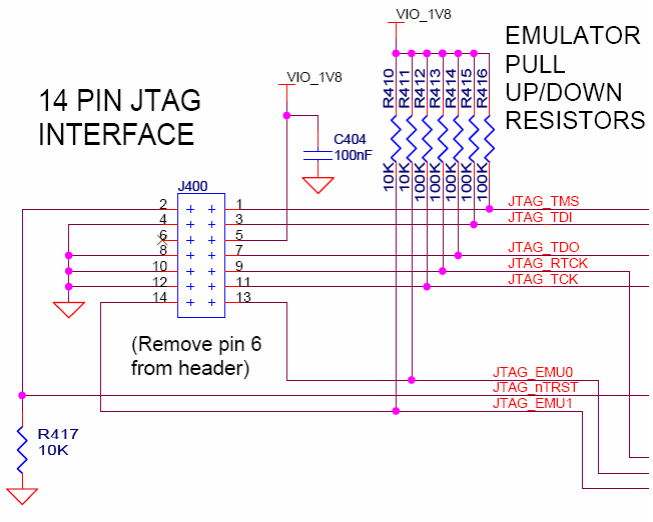


Figure 18 Schematic J400

WARNING: The JTAG signals goes directly to OMAP processor. Improperly use of this connector could result in damage of the processor.

4.3 CONNECTOR J940: POWER + RS485

The J940 connector is a HEADER CONNECTOR PH SIDE 5POS 2MM SMD from JST (Part Number: S5B-PH-SM3-TB)

Pin 1 is labeled on the PCB. The connector is located as shows the figure below.

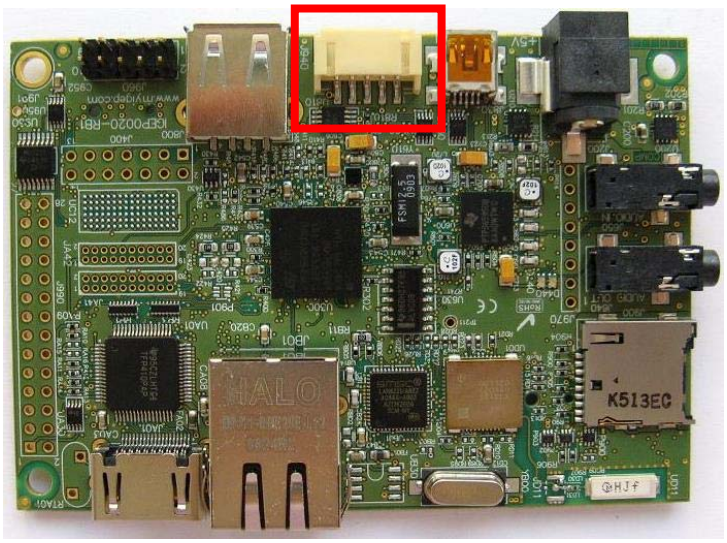


Figure 19 J940 location

The schematic below illustrate the pinout of the connector.

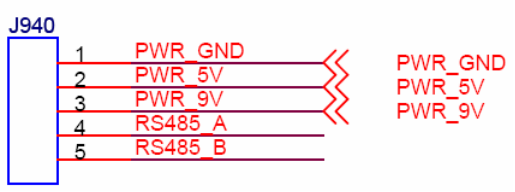


Figure 20 Schematic J940

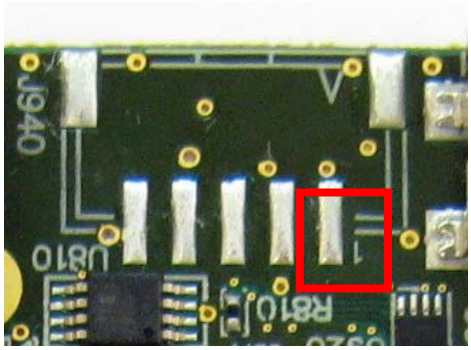


Figure 21 J940 detail pin 1

User can use this connector to power the board with 5VDC. Use only 5V regulated DC.

The PWR_9V input is directly routed to JC01 and J971 connectors. The IGEPv2 BOARD do not use this power supply.

There is also a RS485 interface on the connector.

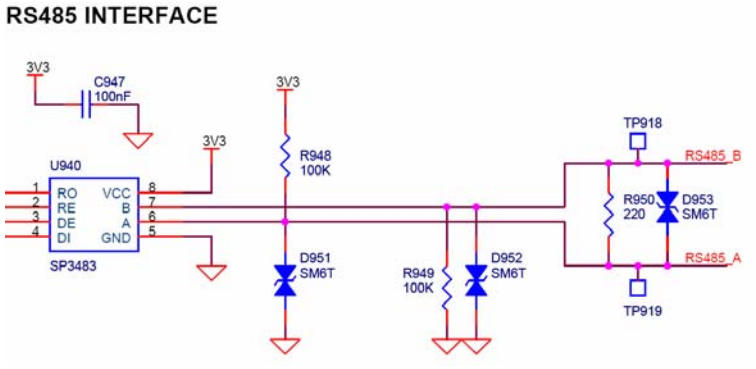


Figure 22 Schematic RS485 driver

4.4 CONNECTOR J960: RS232 SERIAL PORT DEBUG – IDC10

The J960 connector is a 5x2 pins double row 2.54mm.

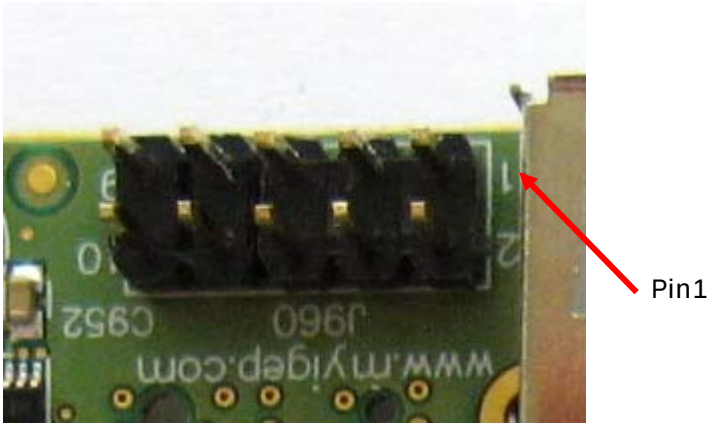


Figure 23 J960 detail

The connector is located as shows the figure below.

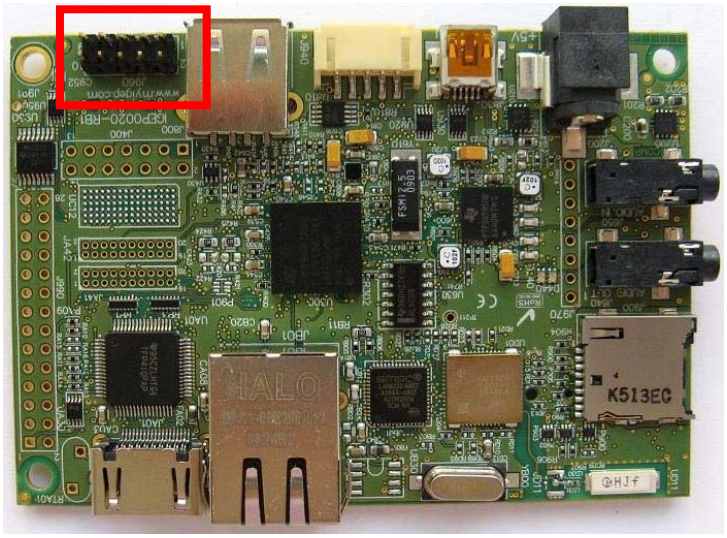


Figure 24 J960 location

The schematic below illustrate the pin out of the connector.

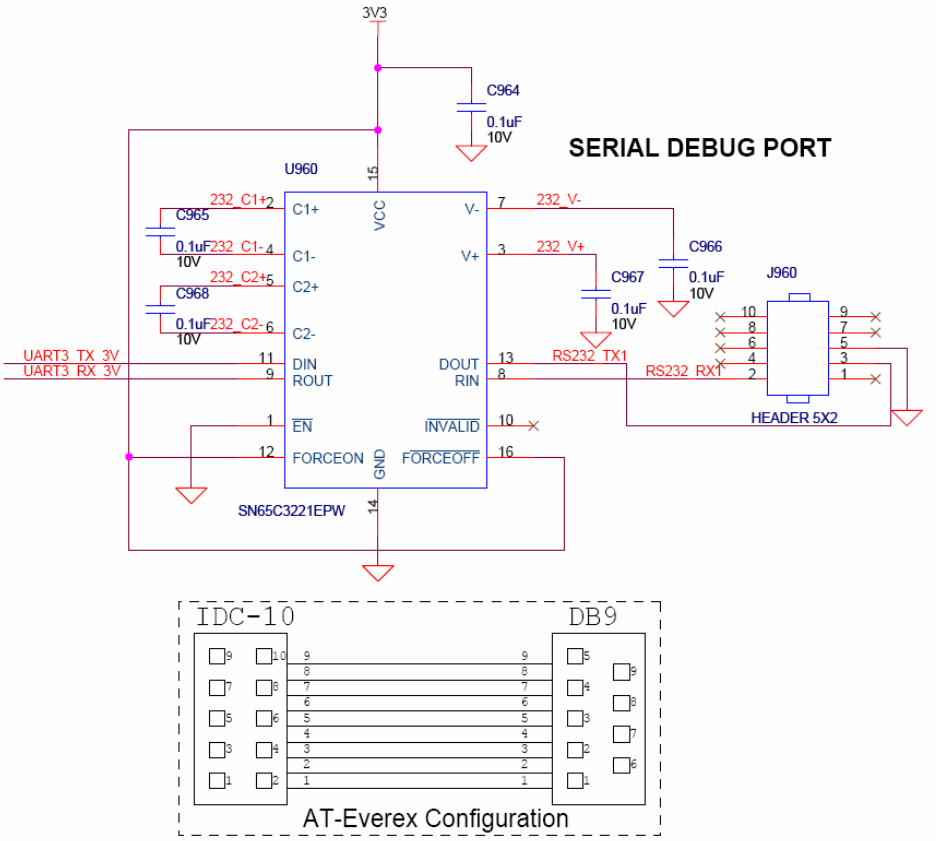


Figure 25 Schematic J960

The 5x2 Header follow the IDC-10 (AT-Everex) configuration.

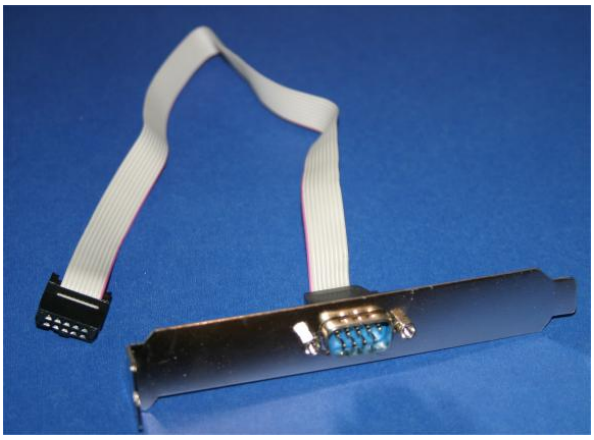


Figure 26 IDC-10 to DB9 cable

4.5 CONNECTOR J971: KEYBOARD MATRIX 4X4

The J971 connector is a 8 pins single row 2.54mm.

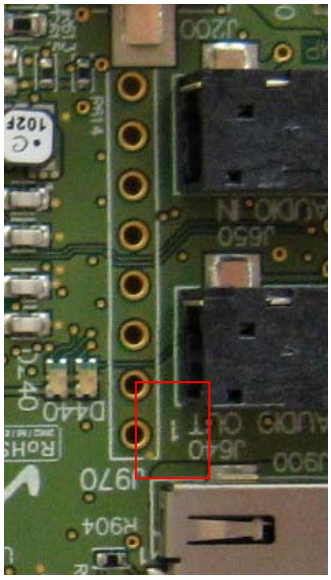


Figure 27 J971 detail

Its can be used to connect a 4x4 keyboard matrix.

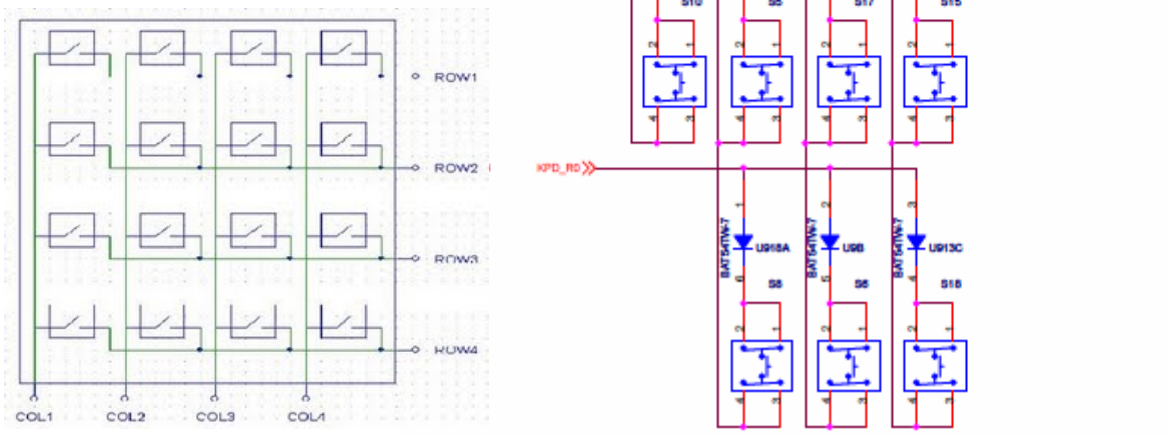


Figure 28 Keyboard matrix 4x4 and schematic example

Pin 1 is labeled on the PCB. The connector is located as shows the figure below.

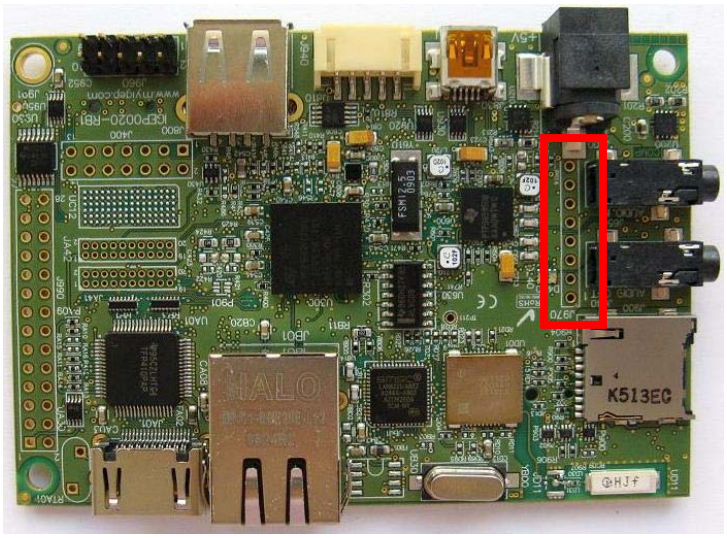


Figure 29 J971 location

The schematic below illustrate the pin out of the connector.

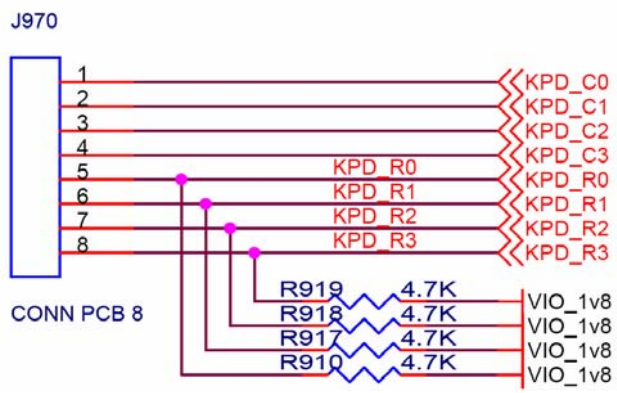


Figure 30 Schematic J971

KPD_Cx: columns

KPD_Rx: rows

When a key button of the keyboard matrix is pressed the corresponding row and column lines are shorted together. To allow key press detection, all input pins (KBR) are pulled up to VCC and all output pins (KBC) driven to a low level.

Any action on a button generates an interrupt to the sequencer.

The decoding sequence is written to allow detection of simultaneous press actions on several key buttons.

4.6 CONNECTOR JA41-JA42: TFT

There are two 1.27mm Double Row Terminal Strip for the TFT interface. Both are from SAMTEC manufacturer (Part Number FTS-110-01-L-D).

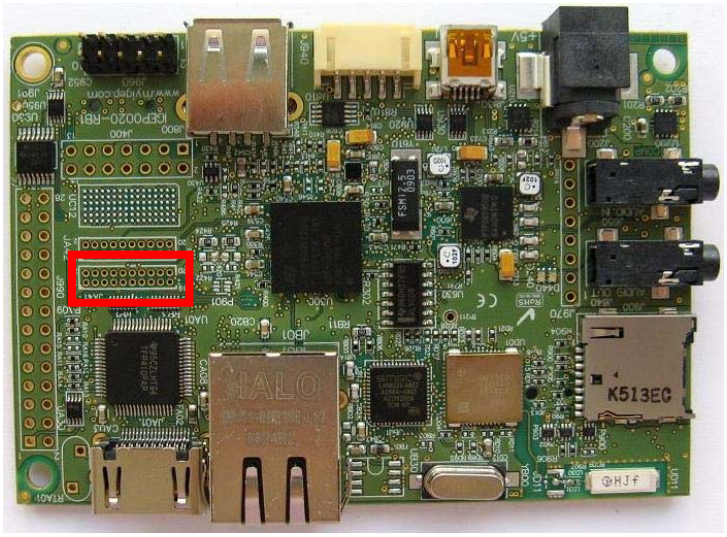


Figure 31 JA41 location

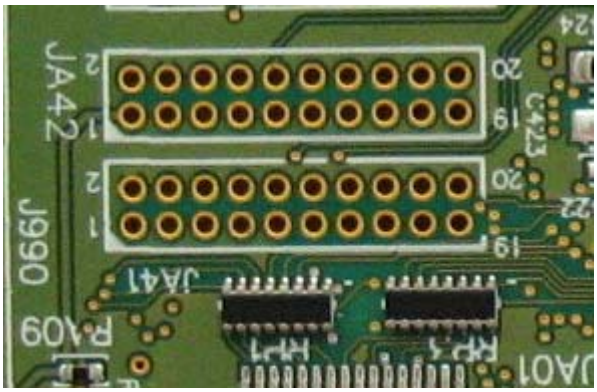


Figure 32 JA41-JA42 detail

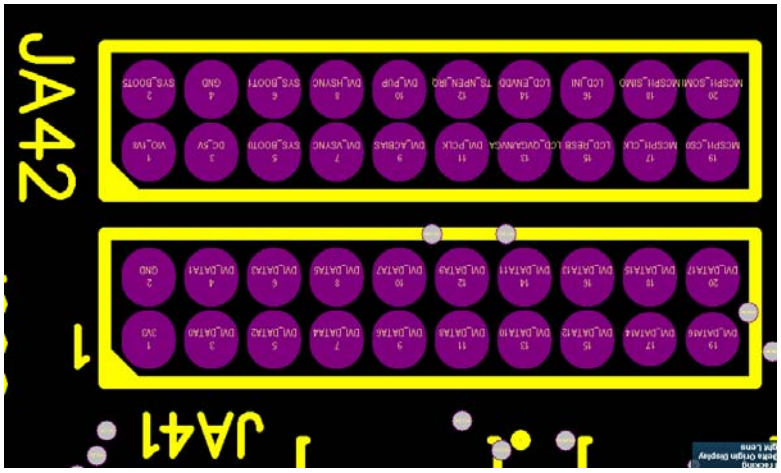


Figure 33 JA41-JA42 pinout detail

This connectors allow the access to the LCD signals. Next table shows the signals that are on the JA41 and JA42 connector.

Pin#	Signal	I/O	Description
1	3V3	PWR	DC rail from the Main DC supply
2	GND	PWR	Ground
3	DVI_DATA0	O	LCD Pixel Data bit
4	DVI_DATA1	O	LCD Pixel Data bit
5	DVI_DATA2	O	LCD Pixel Data bit
6	DVI_DATA3	O	LCD Pixel Data bit
7	DVI_DATA4	O	LCD Pixel Data bit
8	DVI_DATA5	O	LCD Pixel Data bit
9	DVI_DATA6	O	LCD Pixel Data bit
10	DVI_DATA7	O	LCD Pixel Data bit
11	DVI_DATA8	O	LCD Pixel Data bit
12	DVI_DATA9	O	LCD Pixel Data bit
13	DVI_DATA10	O	LCD Pixel Data bit
14	DVI_DATA11	O	LCD Pixel Data bit
15	DVI_DATA12	O	LCD Pixel Data bit
16	DVI_DATA13	O	LCD Pixel Data bit
17	DVI_DATA14	O	LCD Pixel Data bit
18	DVI_DATA15	O	LCD Pixel Data bit
19	DVI_DATA16	O	LCD Pixel Data bit
20	DVI_DATA17	O	LCD Pixel Data bit

Table 1 JA41 connector pinout

This connector can also be used for other functions on the board based on the multiplexer setting of each pin. Next table 22 shows the options. The MUX: column indicates which MUX mode must be set for each pin to make the respective signals accessible on the pins of the OMAP3530.

Signal	MUX:0	MUX:2	MUX:4
DVI_DATA0	DATA0	UART1_CTS	GPIO70

DVI_DATA1	DATA1	UART1_RTS	GPIO71
DVI_DATA2	DATA2	-	GPIO72
DVI_DATA3	DATA3	-	GPIO73
DVI_DATA4	DATA4	UART3_RX	GPIO74
DVI_DATA5	DATA5	UART3_TX	GPIO75
DVI_DATA6	DATA6	UART1_TX	GPIO_76
DVI_DATA7	DATA7	UART1_RX	GPIO_77
DVI_DATA8	DATA8	-	GPIO_78
DVI_DATA9	DATA9	-	GPIO_79
DVI_DATA10	DATA10	-	GPIO79
DVI_DATA11	DATA11	-	GPIO81
DVI_DATA12	DATA12	-	GPIO82
DVI_DATA13	DATA13	-	GPIO83
DVI_DATA14	DATA14	-	GPIO84
DVI_DATA15	DATA15	-	GPIO85
DVI_DATA16	DATA16	-	GPIO86
DVI_DATA17	DATA17	-	GPIO87

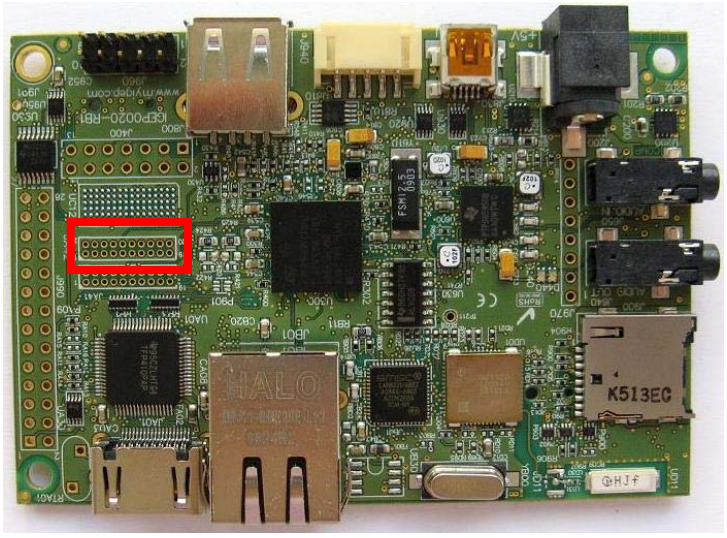


Figure 34 JA42 location

Pin#	Signal	I/O	Description
1	VIO_1V8	PWR	1.8V buffer reference rail.
2	SYS_BOOT5	I	OMAP boot config
3	DC_5V	PWR	5V reference rail.
4	GND	PWR	
5	SYS_BOOT0	I	OMAP boot config
6	SYS_BOOT1	I	OMAP boot config
7	DVI_VSYNC	O	LCD Vertical Sync
8	DVI_HSYNC	O	LCD Horizontal Sync
9	DVI_ACBIAS	O	LCD control
10	DVI_PUP	O	Control signal for the DVI controller. When Hi, DVI is enabled. Can be used to activate circuitry on adapter board if desired.

11	DVI_PCLK	O	LCD clock
12	TS_nPEN_IRQ	O	Touchscreen control
13	LCD_QVGA/nVGA	O	Touchscreen control
14	TS_ENVVDD	O	Touchscreen control
15	LCD_RESB	O	Touchscreen control
16	LCD_INI	O	Touchscreen control
17	MCSPI1_CLK	O	Touchscreen control
18	MCSPI1_SIMO	I	Touchscreen control
19	MCSPI1_CS0	O	Touchscreen control
20	MCSPI1_SOMI	O	Touchscreen control

Table 2 JA42 connector pinout

The current available on the DC_5V rail is limited to the available current that remains from the DC supply that is connected to the DC power jack on the board. Keep in mind that some of that power is needed by the USB Host power rail and if more power is needed for the expansion board, the main DC power supply current capability may need to be increased. All signals are 1.8V except the DVI_PUP which is a 3.3V signal.

The 1.8V rail is for level translation only and should not be used to power circuitry on the board. The 3.3V rail also has limited capacity on the power as well.

It is suggested that the 5V rail be used to generate the required voltages for an adapter card.

The schematic below illustrate the pin out of the connectors.

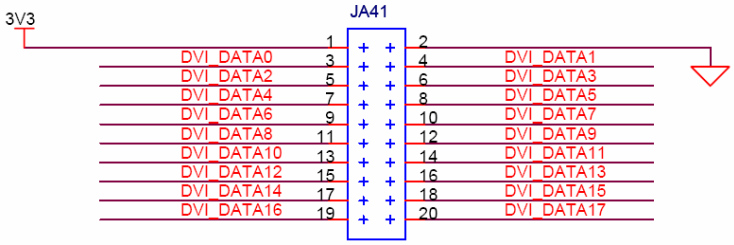


Figure 35 Schematic JA41

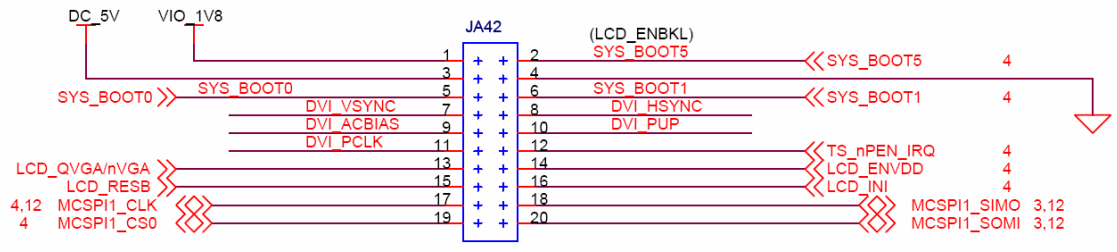


Figure 36 Schematic JA2

JA41 and JA42 connectors are NOT BeagleBoard compatible.

4.7 CONNECTOR J990: GPIO

The J990 connector is a 28 pins 2x14 dual row 2.54mm.

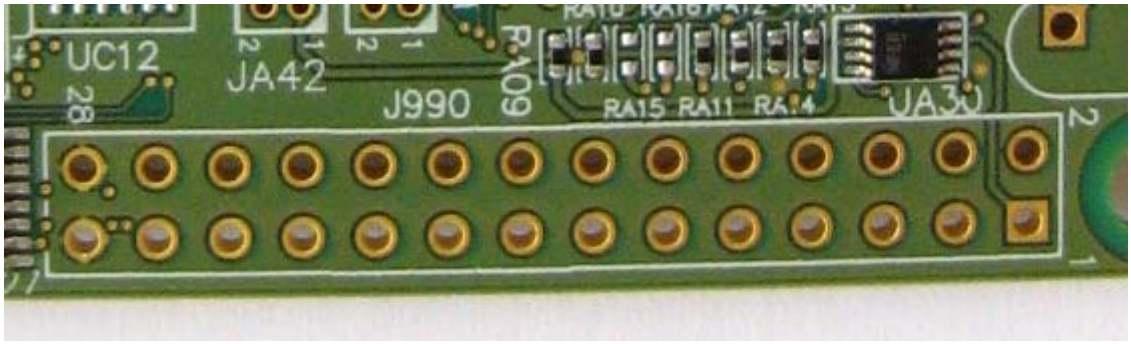


Figure 37 J990 detail

Pins 1, 2, 27 and 28 are labeled on PCB.

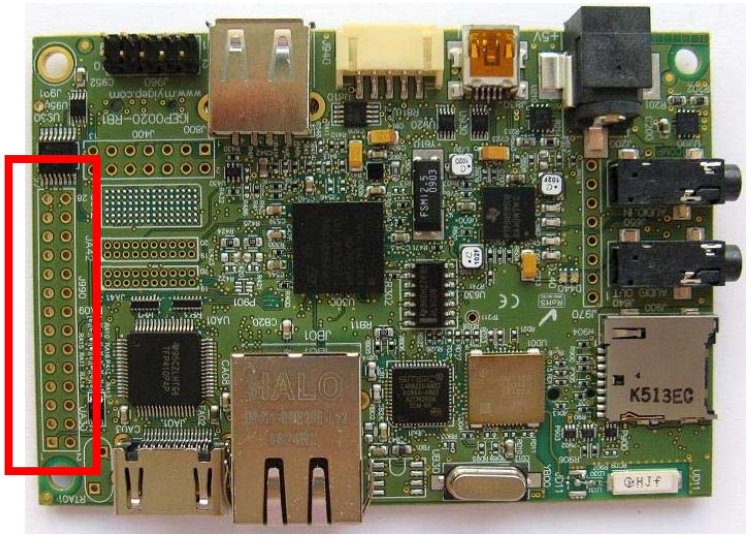


Figure 38 J990 location

The schematic below illustrate the pin out of the connectors.

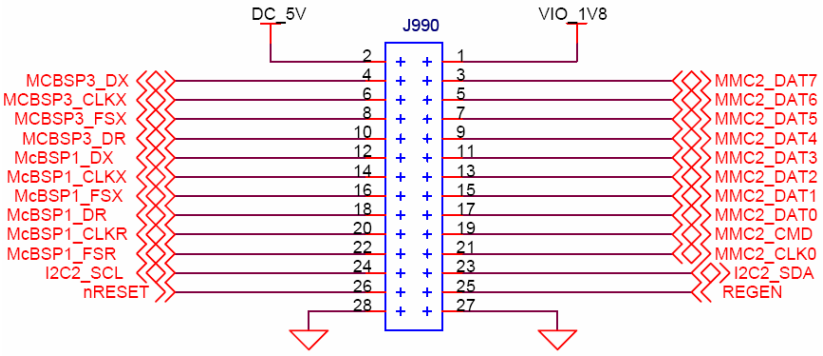


Figure 39 Schematic J990

Pin 1, 2, 27 and 28 are labeled on the PCB.

Using this expansion connector you have access to McBSP1, McBSP3, I2C2, MMC2 (8 bits), nReset and REGEN signals from OMAP Processor. The interface is at 1.8V on all signals. Only 1.8V CMOS levels are supported. **DO NOT expose the header to 3.3V.**

J990 connector is BeagleBoard (http://beagleboard.org) expansion connector compatible.

Pin	MUX:0	MUX:1	MUX:2	MUX:4
1	VIO_1V8			
2	DC_5V			
3	MMC2_DAT7			GPIO_139
4	McBSP3_DX	UART2_CTS		GPIO_140
	UART2_CTS	McBSP3_DX	GPT9_PWMEVT	GPIO_144
5	MMC2_DAT6			GPIO_138
6	McBSP3_CLKX	UART2_TX		GPIO_142
	UART2_TX	McBSP3_CLKX	GPT11_PWMEVT	GPIO_146
7	MMC2_DAT5			GPIO_137
8	McBSP3_FSX	UART2_RX		GPIO_143
9	MMC2_DAT4			GPIO_136
10	McBSP3_DR	UART2_RTS		GPIO_141
	UART2_RTS	McBSP3_DR	GPT10_PWMEVT	GPIO_145
11	MMC2_DAT3	McSPI3_CS0		GPIO_135
12	McBSP1_DX	McSPI4_SIMO	McBSP3_DX	GPIO_158
13	MMC2_DAT2	McSPI3_CS1		GPIO_134
14	McBSP1_CLKX		McBSP3_CLKX	GPIO_162
15	MMC2_DAT1			GPIO_133
16	McBSP1_FSX	McSPI4_CS0	McBSP3_FSX	GPIO_161
17	MMC2_DAT0	McSPI3_SOMI		GPIO_132
18	McBSP1_DR	McSPI4_SOMI	McBSP3_DR	GPIO_159
19	MMC2_CMD	McSPI3_SIMO		GPIO_131
20	McBSP1_CLKR	McSPI4_CLK		GPIO_156

21	MMC2_CLKO	McSPI3_CLK		GPIO_130
22	McBSP1_FSR			GPIO_157
23	I2C2_SDA	GPIO_183		
24	I2C2_SCL	GPIO_168		
25	REGEN			
26	nRESET			
27	GND			
28	GND			

Table 3 Expansion Connector signals

If you use these signals in their respective groups and that is the only function you use, all of the signals are available. Whether or not the signals you need are all available, depends on the muxing function on a per-pin basis. Only one signal per pin is available at any one time.

Signal	Description	I/O	Pin
SD/MMC Port 2			
MMC2_DAT7	SD/MMC data pin 7.	I/O	3
MMC2_DAT6	SD/MMC data pin 6.	I/O	5
MMC2_DAT5	SD/MMC data pin 5.	I/O	7
MMC2_DAT4	SD/MMC data pin 4.	I/O	9
MMC2_DAT3	SD/MMC data pin 3.	I/O	11
MMC2_DAT2	SD/MMC data pin 2.	I/O	13
MMC2_DAT1	SD/MMC data pin 1.	I/O	15
MMC2_DAT0	SD/MMC data pin 0.	I/O	17
MMC2_CMD	SD/MMC command signal.	I/O	19
MMC_CLKO	SD/MMC clock signal.	O	21
McBSP Port 1			
McBSP1_DR	Multi channel buffered serial port receive	I	18
McBSP1_CLKS	----------	N/A	N/A
McBSP1_FSR	Multi channel buffered serial port transmit frame sync RCV	I/O	22
McBSP1_DX	Multi channel buffered serial port transmit	I/O	12
McBSP1_CLKX	Multi channel buffered serial port transmit clock	I/O	14
McBSP1_FSX	Multi channel buffered serial port transmit frame sync XMT	I/O	16
McBSP1_CLKR	Multi channel buffered serial port receive clock	I/O	20
I2C Port 2			
I2C2_SDA	I2C data line.	IOD	23
I2C2_SCL	I2C clock line	IOD	24
McBSP Port 3			
McBSP3_DR	Multi channel buffered serial port receive	I	10,18
McBSP3_DX	Multi channel buffered serial port transmit	I/O	4,12
McBSP3_CLKX	Multi channel buffered serial port receive clock	I/O	6,14
McBSP3_FSX	Multi channel buffered serial port frame sync transmit	I/O	8,16
General Purpose I/O Pins			
GPIO_130	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	21
GPIO_131	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	19
GPIO_132	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	17
GPIO_133	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	15
GPIO_134	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	13

GPIO_135	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	11
GPIO_136	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	9
GPIO_137	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	7
GPIO_138	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	5
GPIO_139	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	3
GPIO_140	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	4
GPIO_141	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	10
GPIO_142	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	6
GPIO_143	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	8
GPIO_156	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	20
GPIO_158	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	12
GPIO_159	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	18
GPIO_161	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	16
GPIO_162	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	14
GPIO_168	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	24
GPIO_183	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	23
GPIO_144	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	4
GPIO_146	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	6
GPIO_145	General Purpose Input/Output pin. Can be used as an interrupt pin.	I/O	10
McSPI Port 3			
McSPI3_CS0	Multi channel SPI chip select 0	O	11
McSPI3_CS1	Multi channel SPI chip select 1	O	13
McSPI3_SIMO	Multi channel SPI slave in master out	I/O	19
McSPI3_SOMI	Multi channel SPI slave out master in	I/O	17
McSPI3_CLK	Multi channel SPI clock	I/O	21
McSPI Port 4			
McSPI4_SIMO	Multi channel SPI slave in master out	I/O	12
McSPI4_SOMI	Multi channel SPI slave out master in	I/)	18
McSPI4_CS0	Multi channel SPI chip select 0	O	16
UART Port 2			
UART2_CTS	UART clear to send	I/O	4
UART2_RTS	UART request to send	O	10
UART2_RX	UART receive	I	8
UART2_TX	UART transmit	O	6
GPT_PWM			
GPT9_PWMEVT	PWM or event for GP timer	O	4
GPT11_PWMEVT	PWM or event for GP timer	O	10
GPT10_PWMEVT	PWM or event for GP timer	O	8

Table 4 Expansion Connector signals

4.8 CONNECTOR JD11: EXTERNAL WIFI ANTENNA

The JD11 is a GSC connector for the external WIFI interface. It is a MURATA GSC connector, Part number MM9329-2700RA1.

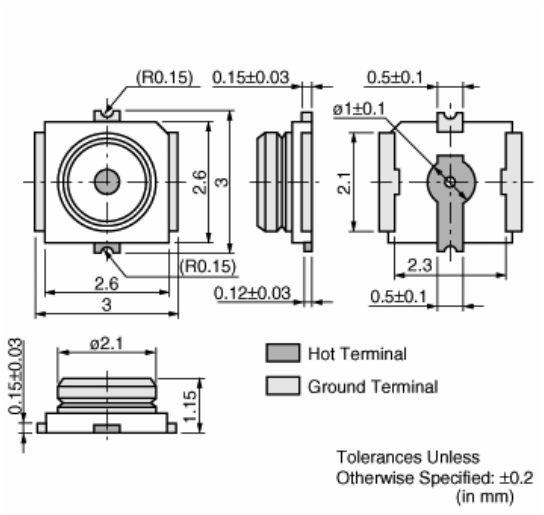


Figure 40 GSC connector specification

Figure 41 JD11 detail

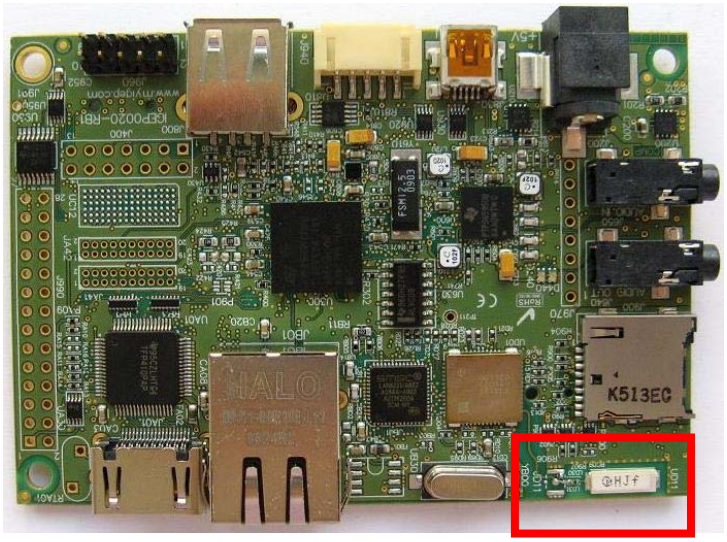


Figure 42 JD11 location

For the cable you will find cable assemblies if you look for CABLE ASSEMBLY RF GSM MURATA to SMA MALE.

4.9 S_VIDEO SIGNALS (TP400 and TP401)

S-video signals are available on TP400 and TP401 test points.

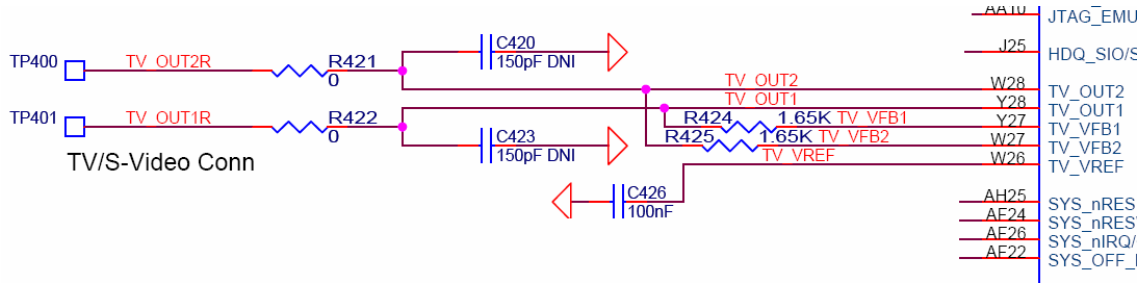


Figure 43 TP400 and TP401 schematic

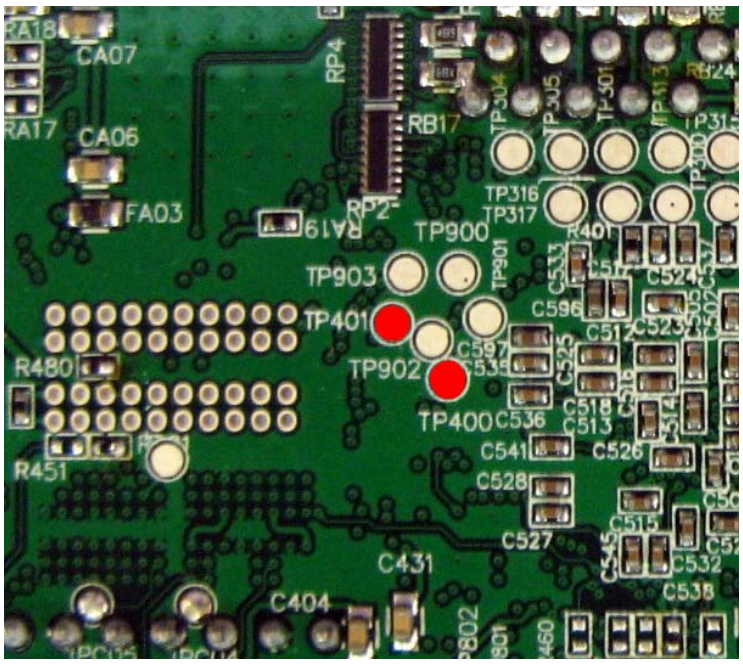


Figure 44 TP400 and TP401 location

4.10 BATTERY BACKUP (R768)

The TPS65950 implements a backup mode, in which the backup battery keeps the RTC running. A rechargeable backup battery can be recharged from the main battery.

When the main battery is below 2.7 V or is removed, the backup battery powers the backup if the backup battery voltage is greater than 1.8 V. The backup domain powers up the following:

- Internal 32.768-kHz oscillator
- RTC
- Hash table (20 registers of 8 bits each)
- Eight GP storage registers

TPS65950 battery backup is available on R768.

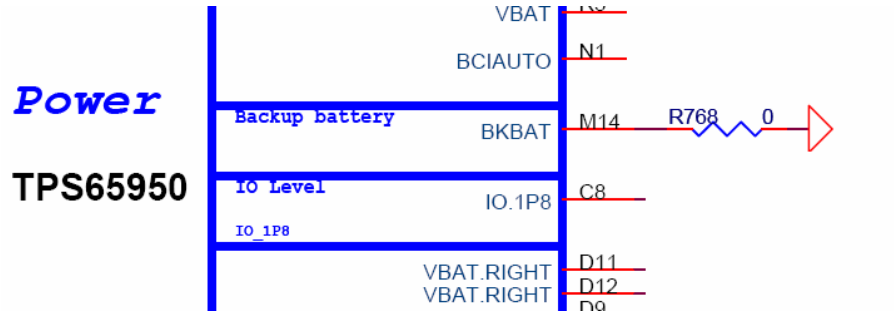


Figure 45 TPS65950 battery backup schematic

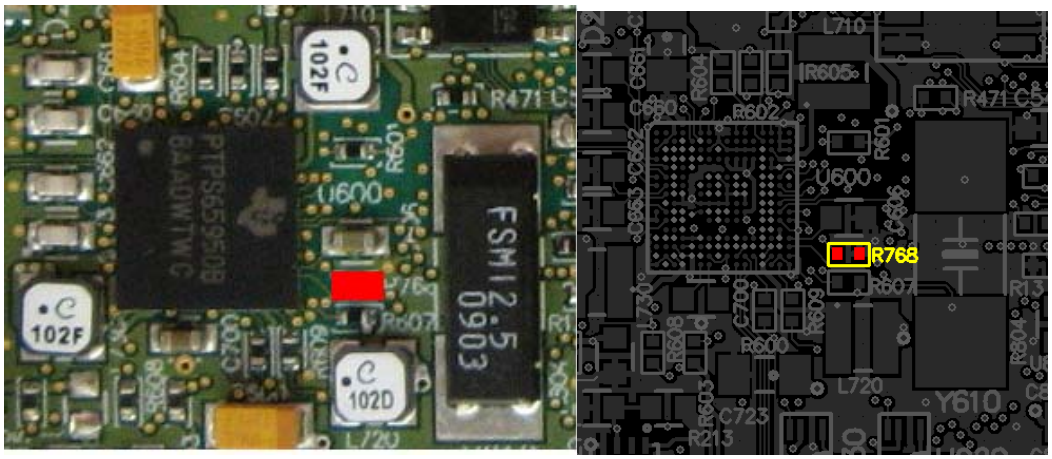


Figure 46 R768 location

5 BOARD REFERENCE

How is IGEPv2 designed?

Product Name: IGEP0020-RB1

Revision ID: RA, RB, Rx (x revision family)

Revision Number: 1, 2, 3 … (n ID revision).

This manual is for Boards designed as IGEP0020-RB1

6 LIST OF FIGURES

Figure 1 POP Package 8

Figure 2 USB OTG connector 9

Figure 3 USB HOST connector 9

Figure 4 ETHERNET connector 10

Figure 5 Stereo Output connector location 10

Figure 6 Stereo Input connector location 11

Figure 7 HDMI connector 12

Figure 8 IGEPv2 BOARD high level block diagram 14

Figure 9 IGEPv2 BOARD top side components 15

Figure 10 IGEPv2 BOARD top side components 15

Figure 11 IGEPv2 BOARD bottom side components 16

Figure 12 IGEPv2 BOARD bottom side components 16

Figure 13 Top view mechanical specification 17

Figure 14 Top view mechanical specification 17

Figure 15 J200 detail 20

Figure 16 J400 detail 21

Figure 17 J400 location 21

Figure 18 Schematic J400 22

Figure 19 J940 location 23

Figure 20 Schematic J940 23

Figure 21 J940 detail pin 1 23

Figure 22 Schematic RS485 driver 23

Figure 23 J960 detail 24

Figure 24 J960 location 24

Figure 25 Schematic J960 25

Figure 26 IDC-10 to DB9 cable 25

Figure 27 J971 detail 26

Figure 28 Keyboard matrix 4x4 and schematic example 26

Figure 29 J971 location 27

Figure 30 Schematic J971 27

Figure 31 JA41 location 28

Figure 32 JA41-JA42 detail 28

Figure 33 JA41-JA42 pinout detail 29

Figure 34 JA42 location 30

Figure 35 Schematic JA41 31

Figure 36 Schematic JA2 31

Figure 37 J990 detail 32

Figure 38 J990 location 32

Figure 39 Schematic J990 33

Figure 41 JD11 detail 36

Figure 42 JD11 location 36

Figure 43 TP400 and TP401 schematic 37

Figure 44 TP400 and TP401 location 37

Figure 45 TPS65950 battery backup schematic 38

Figure 46 R768 location 38

7 CHANGELOG

Revision 1.00 (IGEP-0020-RAx):

- Initial draft

Revision 1.02 (IGEP-0020-RAx):

- Main Memory changed to 4GB/4GB 200 Mhz.

Revision 1.10 (IGEP-0020-RBx):

- This manual applies IGEP-0020-RBx boards.
- Added Wifi+Bluetooth pad for use an external antenna.
- Change LED's location and use low power high intensity leds.
- Add RS-232 transceiver for serial debug, now is compatible with serial debug that use the beagleboard.

Revision 1.11 (IGEP-0020-RBx):

- Mux table on J990 GPIO
- Mux table on JA41-42 : TFT

Revision 1.12 (IGEP-0020-RBx):

- Corrections on mux table on J990 GPIO

Revision 1.13 (IGEP-0020-RBx):

- Note: it is not possible to power the board with the OTG connector.
- Add new chapter: S_VIDEO SIGNALS
- Add new chapter: BATTERY BACKUP
- IGEPv2 board warranty 1 year